1. At what page numbers can you find the information related to 7-segment displays in *DE1-SoC\_User\_Manual.pdf*? To turn on a segment, do you need to apply a high or low logic level?

Answer:

Page 26, and the segment can be turned on or off by applying a low logic level or high logic level from the FPGA. The high level turns on a segment, therefore, a high or low logic level is required to apply.

1. Table 1

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **INPUTS** | |  | **Character** |  |  |  | **OOUTPUTS** | |  |  |
| **D3** | **D2** | **D1** | **D0** | **#** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 6 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | A | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | b | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | c | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | d | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | E | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | F | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inverted Table | **INPUTS** | |  | **Character** |  |  |  | **OOUTPUTS** | |  |  |
| **D3** | **D2** | **D1** | **D0** | **#** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 3 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 7 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 9 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | A | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | b | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | c | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | d | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | E | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | F | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

1. Write the Boolean equation/expression for each of the output found in Table 1 (output a to g). Your solution must be in SOP (Sum of Products) form. Show all your work in deriving your solution by using Minterms. Label your inputs as D3, D2, D1, and D0. Label your outputs as a, b, c, d, e, f, and g.

Answer:

Inverted Expression:

* A = D3’D2’D1’D0 + D3’D2D1’D0’ + D3D2’D1D0 + D3D2D1’D0’ + D3D2D1’D0
* B = D3’D2D1’D0 + D3’D2D1D0’ + D3D2’D1D0 + D3D2D1’D0’ + D3D2D1D0’ + D3D2D1D0
* C = D3’D2’D1D0’ + D3D2D1’D0’ + D3D2D1D0’ + D3D2D1D0
* D = D3’D2’D1’D0 + D3’D2D1’D0’ + D3’D2D1D0 + D3D2’D1’D0 + D3D2’D1D0’ + D3D2D1D0
* E = D3’D2’D1’D0 + D3’D2’D1D0 + D3’D2D1’D0’ + D3’D2D1’D0 + D3’D2D1D0 + D3D2’D1’D0
* F = D3’D2’D1’D0 + D3’D2D1D0 + D3D2D1’D0’ + D3lkoD2D1’D0
* G = D3’D2’D1’D0’ + D3’D2’D1’D0 + D3’D2D1D0

Normal Expression:

* A = D3’D2’D1’D0’+ D3’D2’D1’D0 + D3’D2’D1D0’+ D3’D2’D1D0 + (skip 4) + D3’D2D1’D0 + D3’D2D1D0’+ D3’D2D1D0+ D3D2’D1’D0’+ D3D2’D1’D0 + D3D2’D1D0’ + D3D2D1D0’+ D3D2D1D0
* B= D3’D2’D1’D0’+ D3’D2’D1’D0 + D3’D2’D1D0’+ D3’D2’D1D0 + D3’D2D1’D0’+ (skip 5,6) + D3’D2D1D0 + D3D2’D1’D0’+ D3D2’D1’D0 + D3D2’D1D0’+ D3D2D1’D0
* C= D3’D2’D1’D0’ + D3’D2’D1’D0 + D3’D2’D1D0+ D3’D2D1’D0’ + D3’D2D1’D0 + D3’D2D1D0’ + D3’D2D1D0+ D3D2’D1’D0’ + D3D2’D1’D0+ D3D2’D1D0’ + D3D2’D1D0 + D3D2D1’D0
* D= D3’D2’D1’D0’+(skip 1) + D3’D2’D1D0’+ D3’D2’D1D0 + (skip 4) D3’D2D1’D0 + D3’D2D1D0’+(skip 7) + D3D2’D1’D0’ (skip 9,A) + D3D2’D1D0+ D3D2D1’D0’+ D3D2D1’D0 + D3D2D1D0’
* E= D3’D2’D1’D0’+(skip 1) + D3’D2’D1D0’ + (skip 3,4,5) + D3’D2D1D0’+(skip 7) + D3D2’D1’D0’ (skip 9) + D3D2’D1D0’ + D3D2’D1D0 + D3D2D1’D0’+ D3D2D1’D0 + D3D2D1D0’ + D3D2D1D0
* F= D3’D2’D1’D0’ + (skip 1,2,3) + D3’D2D1’D'0’ + D3’D2D1’D0 + D3’D2D1D0’ + (skip 7) + D3D2’D1’D0’+ D3D2’D1’D0 + D3D2’D1D0’+ D3D2’D1D0 + (skip C,D) + D3D2D1D0’ + D3D2D1D0
* G= (skip 0,1) + D3’D2’D1D0’ + D3’D2’D1D0 + D3’D2D1’D0’ + D3’D2D1’D0 + D3’D2D1D0’ + (skip 7) + D3D2’D1’D0’ + D3D2’D1’D0 + D3D2’D1D0’ + D3D2’D1D0 + D3D2D1’D0’ + D3D2D1’D0 + D3D2D1D0’ + D3D2D1D0

1. Draw the schematic for output **a** using only AND, OR, NOT gates based off your solution from part b.

Answer (Following the inverted expression):

Diagram, schematic

Description automatically generated